UNITRODE

Brushless DC Motor Controller

ADVANCED INFORMATION

FEATURES

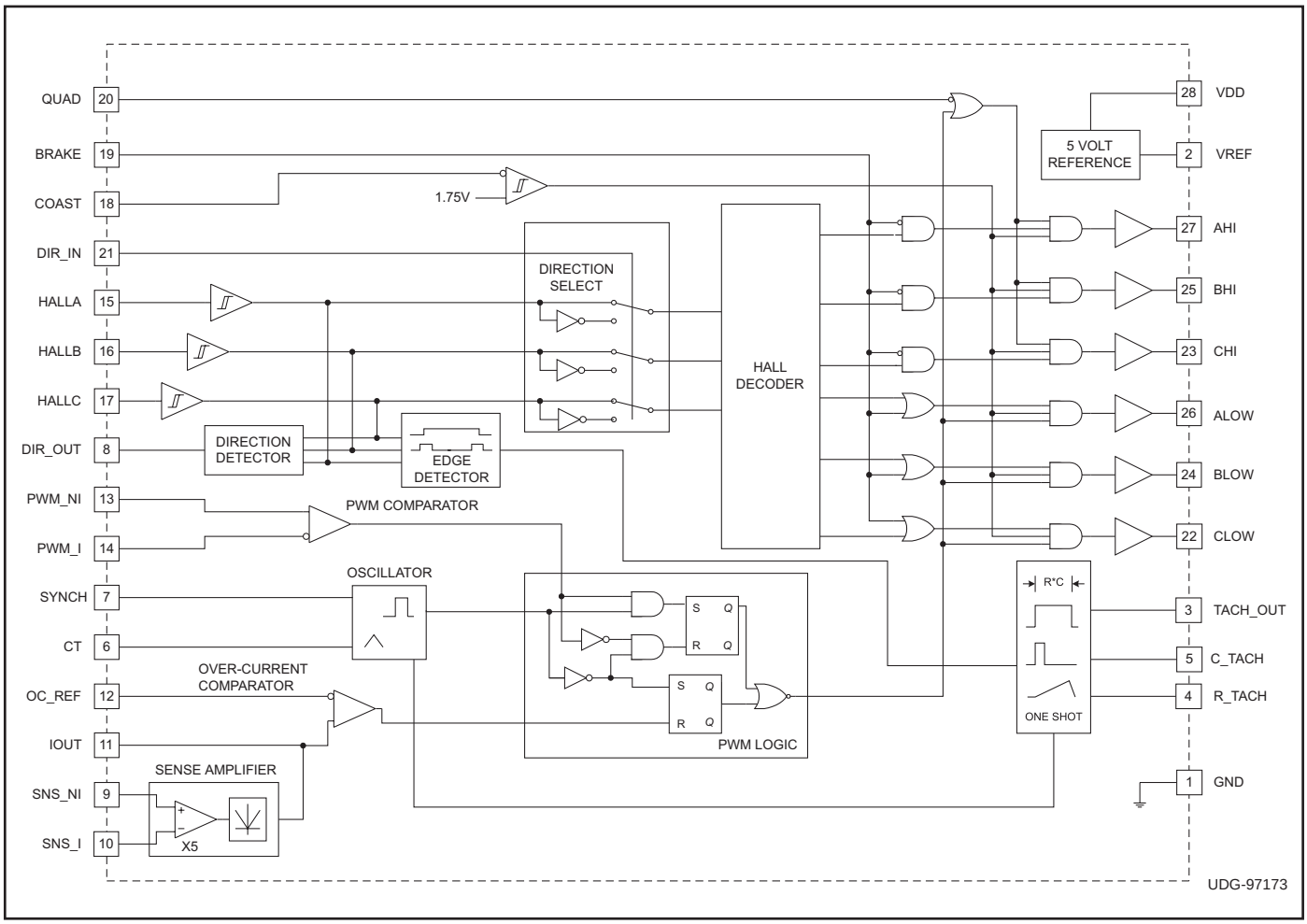
- Two Quadrant and Four Quadrant Operation
- Integrated Absolute Value Current Amplifier
- Pulse-by-Pulse and Average Current Sensing
- Accurate, Variable Duty Cycle Tachometer Output
- Trimmed Precision Reference
- Precision Oscillator
- Direction Output

DESCRIPTION

The UCC3626 motor controller IC combines many of the functions required to design a high performance, two or four quadrant, 3-phase, brushless DC motor controller into one package. Rotor position inputs are decoded to provide six outputs that control an external power stage. A precision triangle oscillator and latched comparator provide PWM motor control in either voltage or current mode configurations. The oscillator is easily synchronized to an external master clock source via the SYNCH input. Additionally, a QUAD select input configures the chip to modulate either the low side switches only, or both upper and lower switches, allowing the user to minimize switching losses in less demanding two quadrant applications.

The chip includes a differential current sense amplifier and absolute value circuit which provide an accurate reconstruction of motor current, useful for pulse by pulse over current protection as well as closing a current control loop. A precision tachometer is also provided for implementing closed loop speed control. The TACH_OUT signal is a variable duty cycle, frequency output which can be used directly for digital control or filtered to provide an analog feedback signal. Other features include COAST, BRAKE, and DIR_IN commands along with a direction output, DIR_OUT.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} . . . . . +15V
Inputs
  Pins 20, 19, 18, 21, 15, 16, 17, 7, 12, 9, 10 . . . . –0.3V to V_{DD}
  Pins 13, 14 . . . . . –0.3V to 7.5V
Output Current
  Pins 22, 23, 24, 25, 26, 27. . . . . 200mA
  Pins 2. . . . . 20mA
  Pins 3. 8, 11 . . . . . 20µA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering 10 Seconds). . . . . +300°C

Note: Unless otherwise indicated, voltages are referenced to ground. Currents are positive into, negative out of specified terminal. Consult packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-28, SOIC-28 (Top View)
J or N Package DW Package

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for VCC = 12V; CT = 1nF, R_{TACH} = 250K, C_{TACH} = 100pF, $T_A = T_J$, T_A = 0°C to 70°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current			3	10	mA
Under-Voltage Lockout					
Start Threshold			10.5		V
UVLO Hysteresis			0.5		V
5.0 V Reference					
Output Voltage	I_{VREF} = –2mA	4.9	5	5.1	V
Line Regulation	11V < VCC < 15V			10	mV
Load Regulation	–1 > I_{VREF} > –5mA			30	mV
Short Circuit Current		40	120		mA
Coast Input Comparator					
Threshold			1.75		V
Hysteresis			0.1		V
Input Bias Current			0.1		µA
Current Sense Amplifier					
Input Offset Voltage	VCM = 0V			5	mV
Input Bias Current	VCM = 0V		5		µA
Input Offset Current	VCM = 0V			0.2	µA
Gain	VCM = 0V	4.9	5	5.1	V/V
CMRR	–0.3V < VCM < 0.5		60		dB
PSRR	11V < VCC <15V		60		dB
Output High Voltage	I_{IOUT} = –100µA	5			V
Output Low Voltage	I_{IOUT} = 100µA			50	mV
Output Source Current	V_{IOUT} = 2V	500			µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for VCC = 12V; CT = 1nF, R_{TACH} = 250K, C_{TACH} = 100pF, $T_A = T_J$, T_A = 0°C to 70°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM Comparator					
Input Offset Voltage	2.5V < VCM = 7.5V			4	mV
Input Bias Current	VCM = 5.0V			0.1	µA
Propogation Delay			75		nS
Over-Current Comparator					
Input Offset Voltage	0V < VCM = 2.5V		6.0		mV
Input Bias Current (OC_REF)	VCM = 0V		–100		nA
Propogation Delay			75		nS
Logic Inputs					
Logic Threshold Voltage	QUAD, BRAKE, DIR	1.5	2.5	3.5	V
Input Current	QUAD, BRAKE, DIR		0.1		µA
Hall Buffer Inputs					
VIL	HALLA, B, C		1		V
VIH	HALLA, B, C		1.9		V
Input Current	0V < V_{IN} < 5V		–25		µA
Oscillator					
Frequency	R_{TACH} = 250k, C_T = 1nF		10		KHz
Frequency Change With Voltage	12V < VCC < 15V			5	%
CT Peak Voltage			7.5		V
CT Valley Voltage			2.5		V
CT Peak-to-Valley Voltage			5.0		V
Tachometer					
V_{OH}/V_{REF}	I_{OUT} = –100µA	98	100	102	%
Vol	I_{OUT} = 100µA		0		V
T-on Accuracy		–3		3	%
Direction Output					
DIR OUT High Level	I_{OUT} = –100µA	3.5		5.1	V
DIR OUT Low Level	I_{OUT} = 100µA	0		1	V
Output Section					
Maximum Duty Cycle				100	%
Output Low Voltage	I_{OUT} = 10mA		0.4		V
Output High Voltage	I_{OUT} = –10mA	4.0		5.1	V
Output Low Voltage	I_{OUT} = 1mA			1	V
Output High Voltage	I_{OUT} = –1mA	4.0		5.1	V
Rise/Fall Time	CI = 100pF		100		nS

PIN DESCRIPTIONS

AHI, BHI, CHI: Digital outputs used to control the high side switches in a three phase inverter. For specific decoding information reference Table I.

ALOW, BLOW, CLOW: Digital outputs used to control the low side switches in a three phase inverter. For specific decoding information reference Table I.

BRAKE: BRAKE is a digital input which causes the device to enter brake mode. In brake mode all three high side outputs are turned off, AHI, BHI & CHI, while all three lowside outputs are turned on, ALOW, BLOW, CLOW. During brake mode the tachometer output remains operational. The only conditions which can inhibit the low side commands during brake are UVLO, exceed-

PIN DESCRIPTIONS (continued)

ing peak current, the output of the PWM comparator, or the COAST command.

COAST: The COAST input consists of a hysteretic comparator which disables the outputs. The input is useful in implementing an overvoltage bus clamp in four quadrant applications. The outputs will be disabled when the input is above 1.75V.

CT: This pin is used in conjunction with the R_TACH pin to set the frequency of the oscillator. A timing capacitor is normally connected between this point and ground and is alternately charged and discharged between 2.5 and 7.5V.

C_TACH: A timing capacitor is connected between this pin and ground to set the width of the TACH_OUT pulse. The capacitor is charged with a current set by the resistor on pin RT.

DIR_IN: DIR_IN is a digital input which determines the order in which the HALLA,B & C inputs are decoded. For specific decode information reference Table I.

DIR_OUT: DIR_OUT represents the actual direction of the rotor as decoded from the HALLA, B & C inputs. For any valid combination of HALLA, B &C inputs there are two valid transitions, one which translates to a clockwise rotation and another which translates to a counterclockwise rotation. The polarity of DIR_OUT is the same as DIR_IN while motoring, i.e. sequencing from top to bottom in Table 1.

GND: GND is the reference ground for all functions of the part. Bypass and timing capacitors should be terminated as close to this point as possible.

HALLA,B,C: These three inputs are designed to accept rotor position information positioned 120° apart. For specific decode information reference Table I. These inputs should be externally pulled-up to VREF or another appropriate external supply.

IOUT: IOUT represents the output of the current sense and absolute value amplifiers. The output signal appearing is a representation of the following expression:

$$I_{OUT} = 2.5V + ABS(ISENS\_I - ISENS\_NI).$$

This output can be used to close a current control loop as well as provide additional filtering of the current sense signal.

OC_REF: OC_REF is an analog input which sets the trip voltage of the overcurrent comparator. The sense input of the comparator is internally connected to the output of the current sense amplifier and absolute value circuit.

PWM_NI: PWM_NI is the noninverting input to the PWM comparator.

PWM_I: PWM_I is the inverting input to the PWM comparator.

QUAD: The QUAD input selects between “two” QUAD = 0 and “four” QUAD = 1 quadrant operation. When in “two-quadrant” mode only the low side devices are effected by the output of the PWM comparator. In “four-quadrant” mode both high and low side devices are controlled by the PWM comparator.

SYNCH: The SYNCH input is used to synchronize the modulator with a master controller or to interface the controller with a digital PWM command signal.

SNS_NI, SNS_I: These inputs are the noninverting and inverting inputs to the current sense amplifier, respectively. The integrated amplifier is configured for a gain of five in addition to providing a 2.5V offset. An absolute value function is also incorporated into the output in order to provide a representation of actual motor current when operating in four quadrant mode.

TACH_OUT: TACH_OUT is the output of a monostable triggered by a change in the commutation state, thus providing a variable duty cycle, frequency output. The on-time of the monostable is set by the timing capacitor connected to C_TACH. The monostable is capable of being retriggered if a commutation occurs during it's on-time.

R_TACH: A resistor connected between R_TACH and ground programs the current for both the oscillator and tachometer.

VDD: VDD is the input supply connection for this device. Undervoltage lockout keeps the outputs off for inputs below 9V. The input should be bypassed with a 0.1uF ceramic capacitor, minimum.

VREF: VREF is a 5V, 1% trimmed reference output with 5 mA of maximum available output current. This pin should be bypassed to ground with a 0.1uF ceramic capacitor, minimum.

APPLICATION INFORMATION

Table 1 provides the decode logic for the six outputs, AHI, BHI, CHI, ALOW, BLOW, and CLOW as a function of the BRAKE, COAST, DIR_IN, HALLA, HALLB, and HALLC inputs.

The UCC3626 is designed to operate with 120° position sensor encoding. In this format, the three position sensor signals are never simultaneously high or low. Motor's whose sensors provide 60° encoding can be converted to 120° using the circuit shown in Figure 1.

BRAKE	COAST	DIR_IN	HALL INPUTS			HIGH SIDE OUTPUTS			LOW SIDE OUTPUTS		
			A	B	C	A	B	C	A	B	C
0	0	1	1	0	1	1	0	0	0	1	0
0	0	1	1	0	0	1	0	0	0	0	1
0	0	1	1	1	0	0	1	0	0	0	1
0	0	1	0	1	0	0	1	0	1	0	0
0	0	1	0	1	1	0	0	1	1	0	0
0	0	1	0	0	1	0	0	1	0	1	0
0	0	0	1	0	1	0	1	0	1	0	0
0	0	0	0	0	1	0	1	0	0	0	1
0	0	0	0	1	1	1	0	0	0	0	1
0	0	0	0	1	0	1	0	0	0	1	0
0	0	0	1	1	0	0	0	1	0	1	0
0	0	0	1	0	0	0	0	1	1	0	0
X	1	X	X	X	X	0	0	0	0	0	0
1	0	X	X	X	X	0	0	0	1	1	1

Table 1. Commutation Truth Table

In order to prevent noise from commanding improper commutation states, some form of low pass filtering on HALLA, HALLB, and HALLC is recommended. Passive RC networks generally work well and should be located as close to the IC as possible. Figure 2 illustrates these techniques.

Configuring the Oscillator

The UCC3626 oscillator is designed to operate at frequencies up to 250kHz and provide a triangle waveform on CT with a peak to peak amplitude of 5 volts for improved noise immunity. The current used to program CT is derived off of the R_TACH resistor according to the following equation:

$$Iosc = \frac{25}{R\_TACH}\ Amps$$

Oscillator frequency is set by R_TACH and CT according to the following relationship:

$$Frequency = \frac{2.5}{(R\_TACH \bullet CT)}\ Hz$$

Timing resistor values should be between 25k and 500k while capacitor values should fall between 100pF and

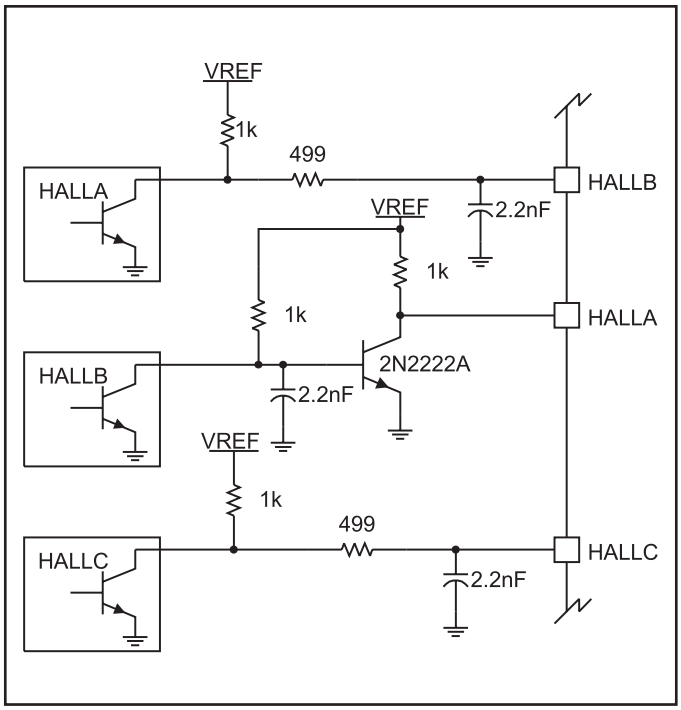


Figure 1.
Circuit to Convert 60° Hall Code to 120° Code

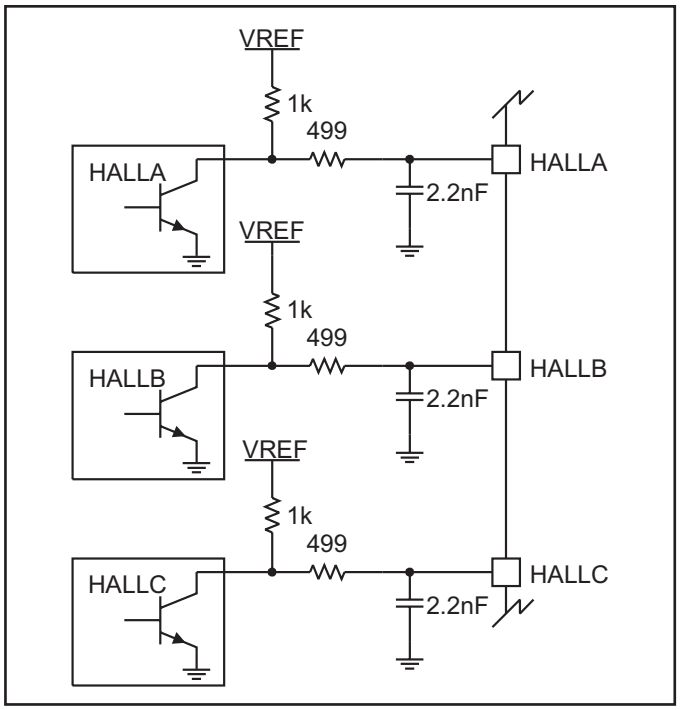


Figure 2. Passive Hall Filtering Technique

1µF. Figure 4 provides a graph of oscillator frequency for various combinations of timing components. As with any high frequency oscillator, timing components should be located as close to the IC pins as possible when laying out the printed circuit board. It is also important to reference the timing capacitor directly to the ground pin on the UCC3626 rather than daisy chaining it to another trace or the ground plane. This technique prevents switching current spikes in the local ground from causing jitter in the oscillator.

Synchronizing the Oscillator

A common system specification is for all oscillators in a design to be synchronized to a master clock. The UCC3626 provides a SYNCH input for exactly this purpose. The SYNCH input is designed to interface with a digital clock pulse generated by the master oscillator. A positive going edge on this input causes the UCC3626 oscillator to begin discharging. In order for the oscillator to function properly it must be programmed for a frequency slightly lower than that of the master. Figure 3 illustrates the waveforms for an oscillator programmed to 20kHz with a master frequency of 30kHz.

Programming the Tachometer

The UCC3626 tachometer consists of a precision, 5V monostable, triggered by either a rising or falling edge on any of the three Hall inputs, HALLA, HALLB, HALLC. The resulting TACH_OUT waveform is a variable dutycycle square wave whose frequency is proportional to motor speed, as given by:

$$TACH\_OUT = \frac{(V \bullet P)}{20} Hz$$

where P is the number of motor pole pairs and V is motor velocity in RPM.

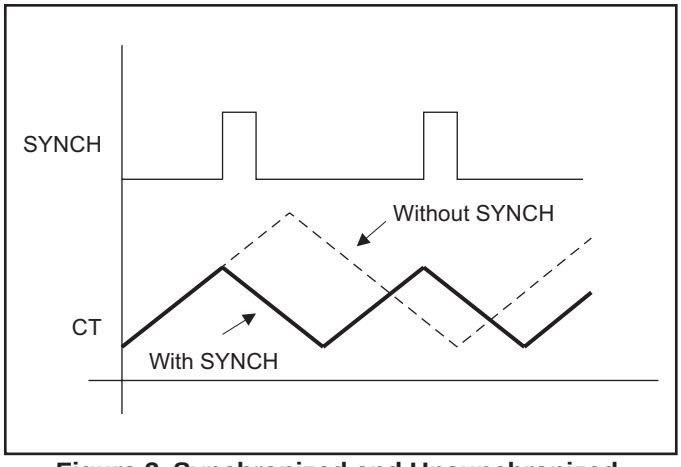


Figure 3. Synchronized and Unsynchronized Oscillator Waveforms

The on-time of the monostable is programmed via timing resistor R_TACH and capacitor C_TACH according to the following equation:

$$On - Time = R\_TACH \bullet C\_TACH \text{sec}$$

Figure 5 provides a graph of On-Time for various combinations of R_TACH and C_TACH. On-Time is typically set to a value less than the minimum TACH-OUT period as given by:

$$T\_Period_{MIN} = \frac{20}{V_{MAX} \bullet P} \text{sec}$$

where P is the number of motor pole pairs and V is motor velocity in RPM.

The TACH_OUT signal can be used to close a digital velocity loop using a microcontroller, as shown in Figure 6, or directly low pass filtered in an analog implementation, Figure 7.

Two Quadrant vs Four Quadrant Control

Figure 8 illustrates the four possible quadrants of operation for a motor. Two quadrant control refers to a system whose operation is limited to quadrants I and III where torque and velocity are in the same direction. With a two quadrant brushless DC amplifier, there are no provisions other than friction to decelerate the load, limiting the approach to less demanding applications. Four quadrant controllers, on the other hand, provide controlled operation in all quadrants, including II and IV, where torque and rotation are of opposite direction.

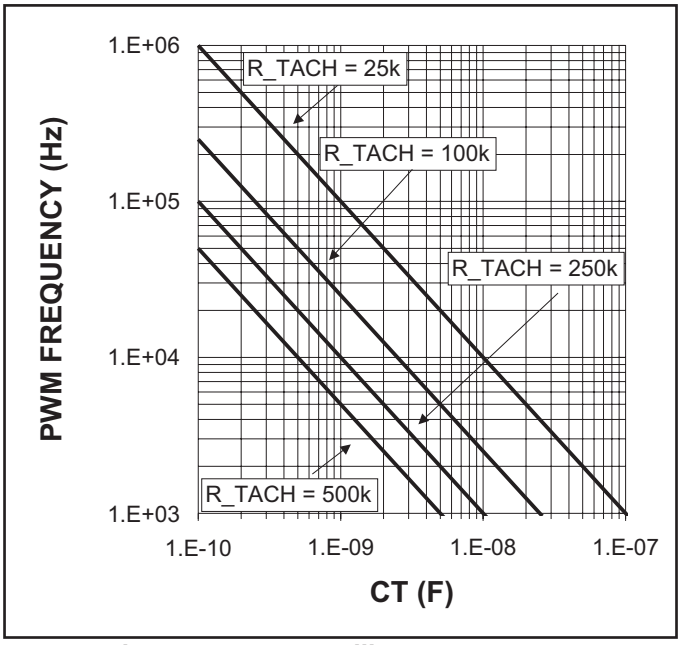


Figure 4. PWM Oscillator Frequency vs. CT and R_TACH

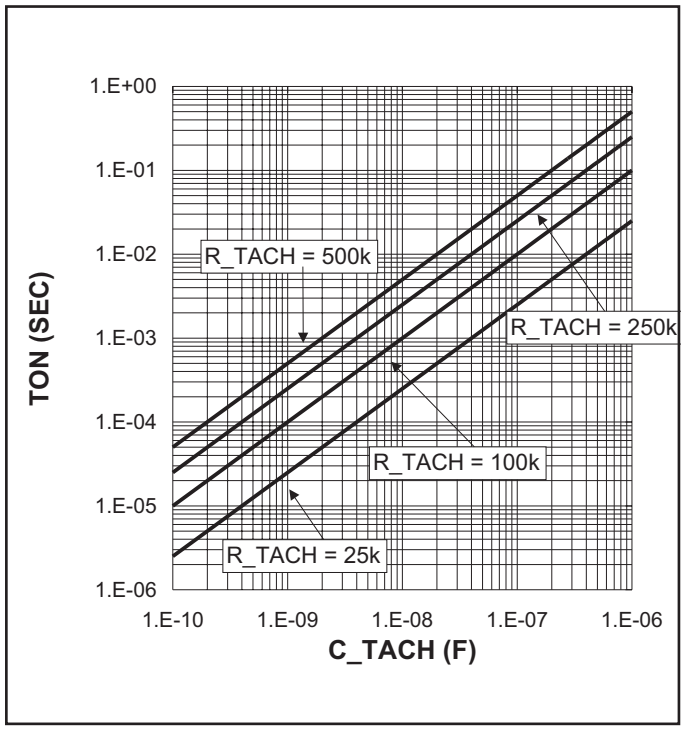


Figure 5. Tachometer On-Time vs. C_TACH and R_TACH

When configured for two quadrant operation, (QUAD=0), the UCC3626 will only modulate the low side devices of the output power stage. The current paths within the output stage during the PWM on and off times are illustrated in Figure 9. During the 'on' interval, both switches are on and current flows through the load down to ground. During the 'off' time, the lower switch is shut off and the motor current circulates through the upper half bridge via the flyback diode. The motor is assumed to be operating in either quadrant I or III.

If one attempts to operate in quadrants II or IV by changing the DIR bit and reversing the torque, switches 1 and 4 are turned off and switches 2 and 3 turned on. Under this condition motor current will very quickly decay, reverse direction and increase until the control threshold is reached. At this point switch 2 will turn off and current will once again circulate in the upper half bridge, however, in this case the motor's BEMF is in phase with the current, i.e. the motor's direction of rotation has not yet changed. Figure 10 illustrates the current paths when operating in this mode. Under these conditions there is nothing to limit the current other than motor and drive impedance. These high circulating currents can result in damage to the power devices in addition to high, uncontrolled torque.

By pulse width modulating both the upper and lower power devices (QUAD=1), motor current will always de-

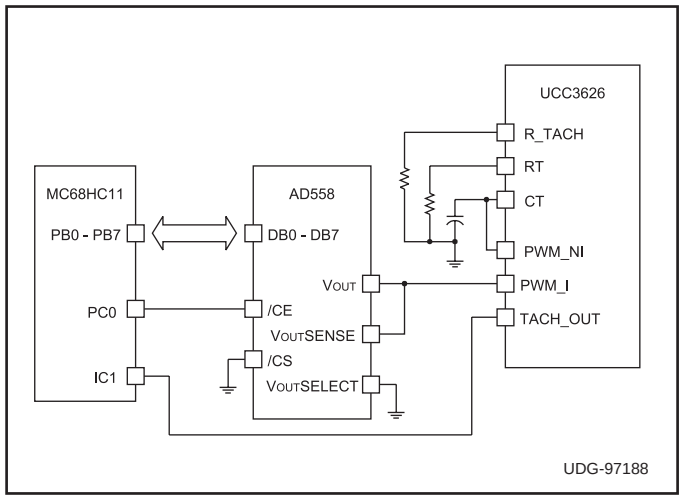


Figure 6: Digital Velocity Loop Implementation

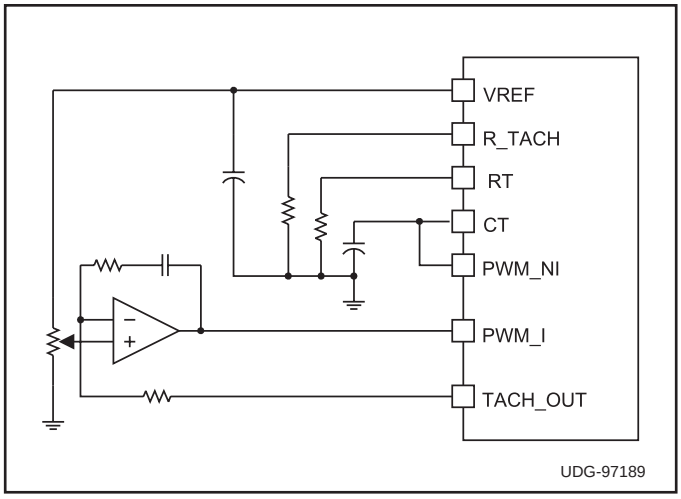


Figure 7: Simple Analog Velocity Loop

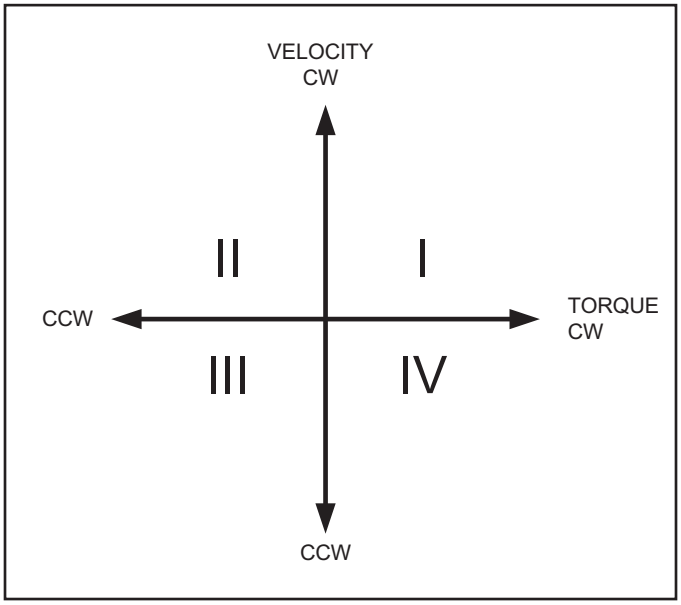


Figure 8: Four Quadrants of Operation

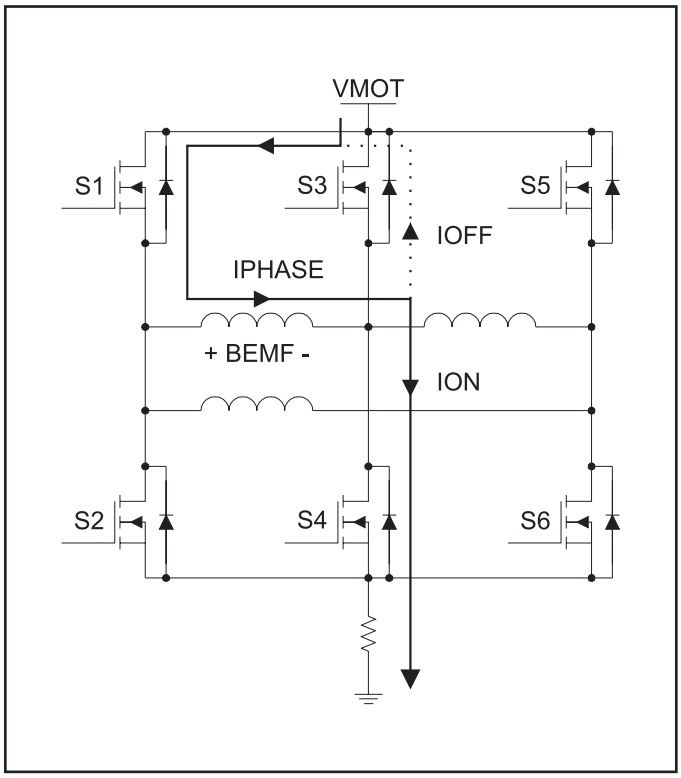


Figure 9: Two Quadrant Chopping

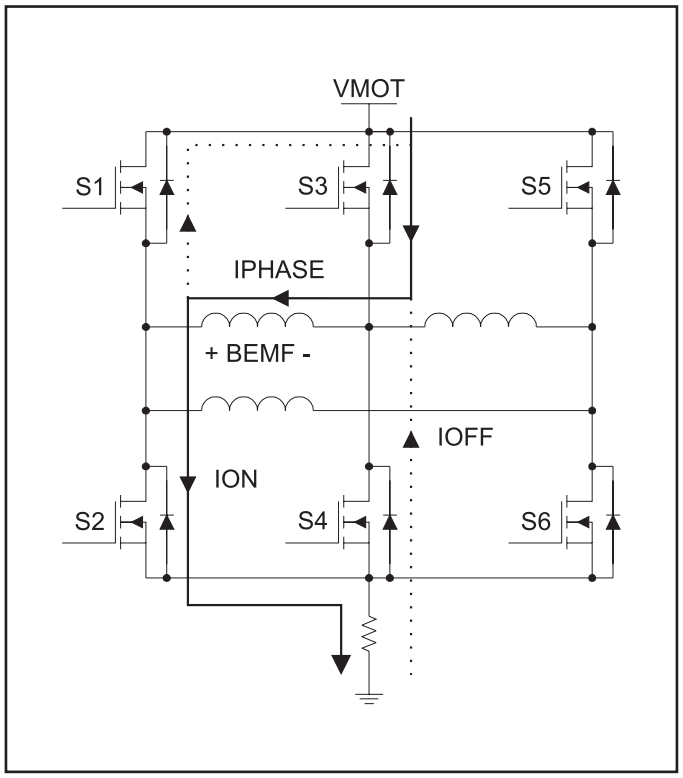


Figure 11: Four Quadrant Reversal

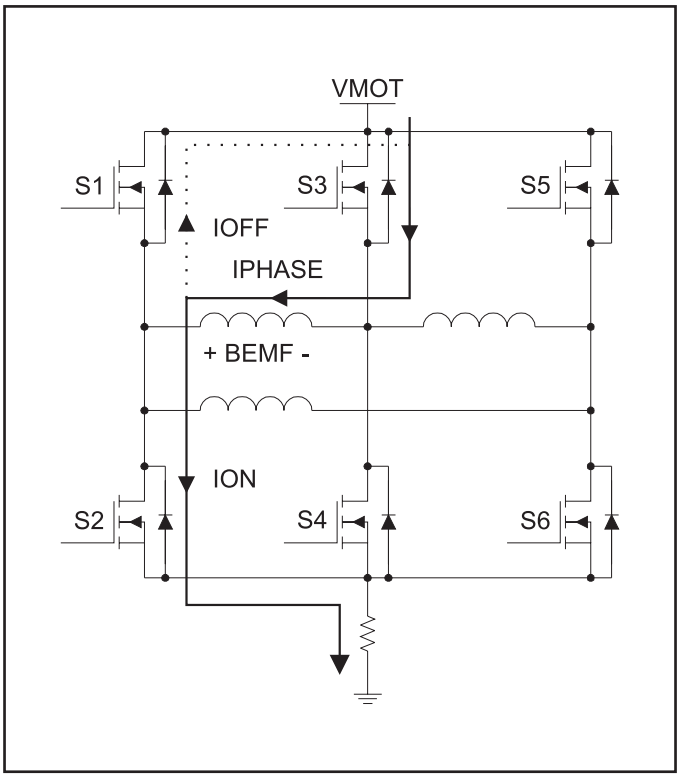


Figure 10: Two Quadrant Reversal

cay during the PWM 'off' time, eliminating any uncontrolled circulating currents. In addition, current will always flow through the current sense resistor, thus providing a suitable feedback signal. Figure 11 illustrates the current paths during a four quadrant torque reversal. Motor drive waveforms for both two and four quadrant operation are illustrated in Figure 12.

Power Stage Design Considerations

The flexible architecture of the UCC3626 requires the user to pay close attention to the design of the power output stage. Two and Four Quadrant applications that do not require the brake function are able to utilize the power stage approach illustrated in Figure 13A. In many cases the body diode of the MOSFET can be utilized to reduce parts count and cost. If efficiency is a key requirement, Schottkey diodes can be used in parallel with the switches.

If the system requires a braking function, diodes must be added in series with the lower power devices and the lower flyback diodes returned to ground, as pictured in Figures 13B,C. This requirement prevents brake currents from circulating in the lower half bridge and bypassing the sense resistor. In addition, the combination of braking and four quadrant control necessitates an additional resistor in the diode path to sense current during the PWM 'off' time as illustrated in Figure 13C.

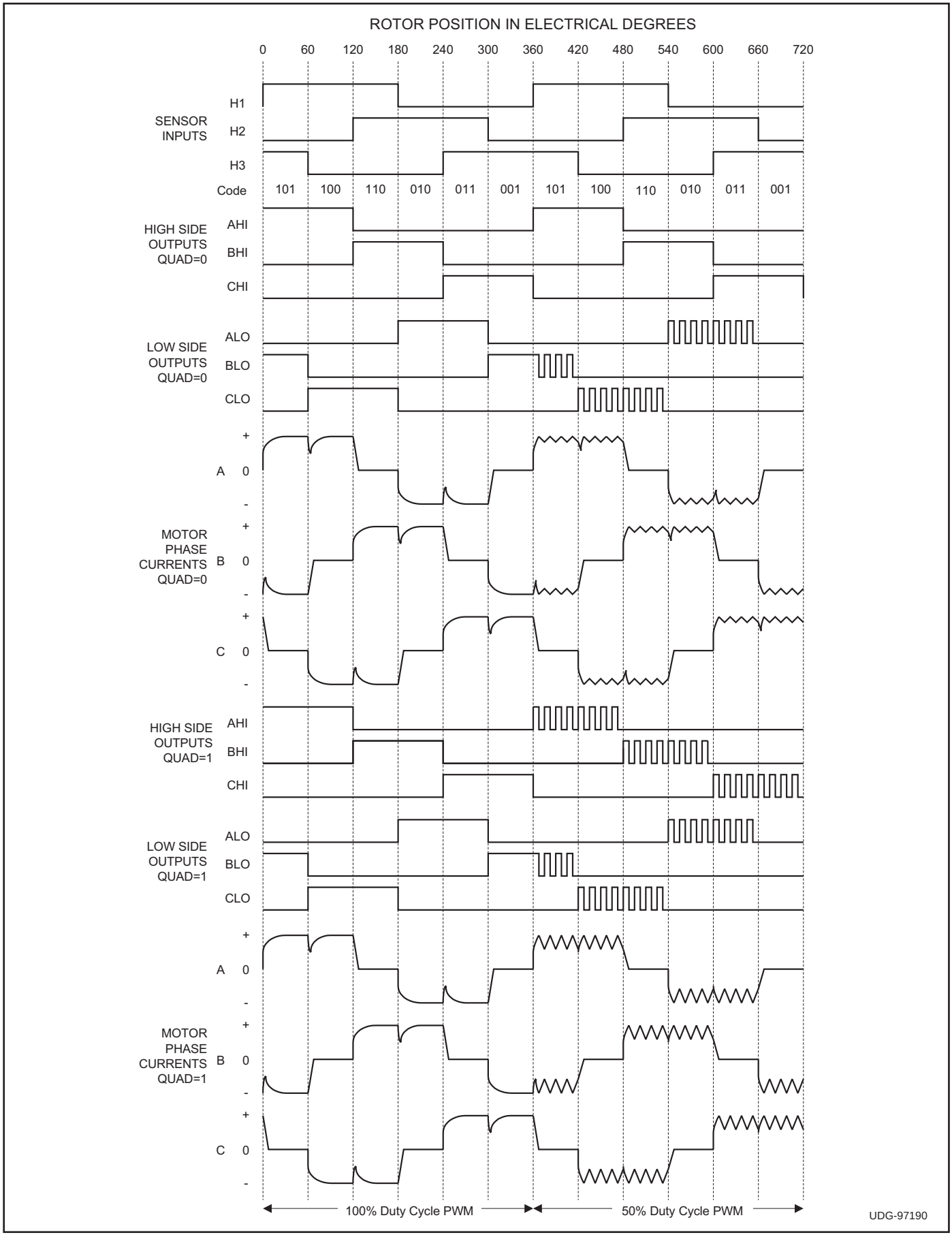


Figure 12: Motor Drive and Current Waveforms for 2 Quadrant (QUAD=0) and 4 Quadrant (QUAD=1) Operation

Current Sensing

The UCC3626 includes a differential current sense amplifier with a fixed gain of five, along with an absolute value circuit. The current sense signal should be low pass filtered to eliminate leading edge spikes. In order to maximize performance, the input impedance of the amplifier should be balanced. If the sense voltage must be trimmed for accuracy reasons, a low value input divider or a differential divider should be used to maintain impedance matching, as shown in Figure 14.

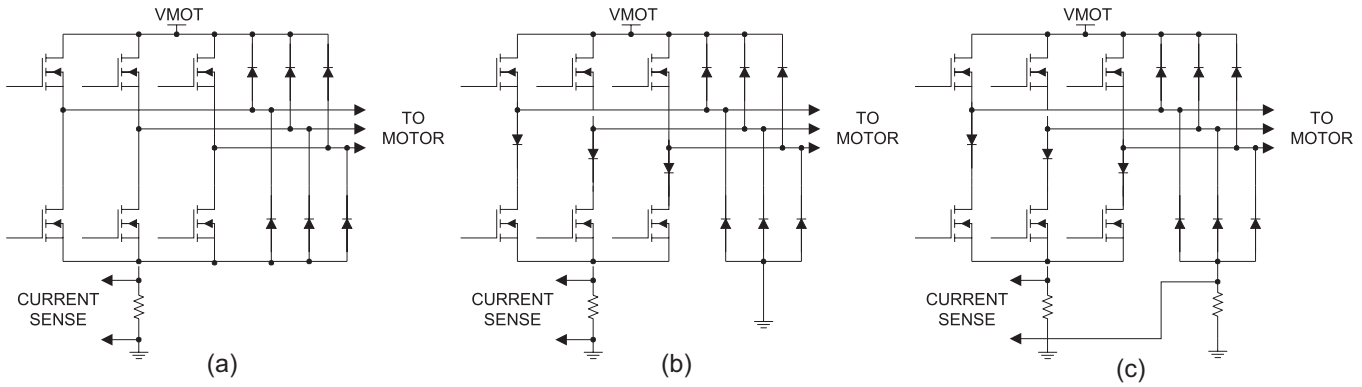
With four quadrant chopping motor current always flows through the sense resistor. However, during the flyback period the polarity across the sense resistor is reversed. The absolute value amplifier cancels the polarity reversal by inverting the negative sense signal during the flyback time, see Figure 15. Therefore, the output of the absolute value amplifier is a reconstructed analog of the motor current, suitable for protection as well as feedback loop closure.

TYPICAL APPLICATIONS

Figure 17 illustrates a simple 175V, 2A two quadrant velocity controller using the UCC3626. The power stage is designed to operate with a rectified off-line supply using IR2210s to provide the interface between the low voltage control signals and the power MOSFETs. The power topology illustrated in Figure 13D is implemented in order to provide braking capability.

The controller's speed command is set by potentiometer R30 while the speed feedback signal is obtained by low pass filtering and buffering the TACH-OUT signal using R11 and C9. Small signal compensation of the velocity control loop is provided by amplifier U5A, whose output is used to control the PWM duty cycle. The integrating capacitor, C8, places a pole at 0Hz and a zero in conjunction with R10. This zero can be used to cancel the low frequency motor pole and cross the loop over with a -20dB gain response.

Four quadrant applications require the control of motor current. Figure 16 illustrates a sign/magnitude current control loop within an outer bipolar velocity loop using the UCC3626. U1 serves as the velocity loop error amplifier and accepts a +/-5V command signal. Velocity feedback is provided by low pass filtering and scaling the TACH_OUT signal using U2. The direction output, DIR_OUT, switch and U3 set the polarity of the tachometer gain according to the direction of rotation. The output of the velocity error amplifier, U1, is then converted to sign/magnitude form using U4, 5, 6 and 7. The sign portion is used to drive the DIR input while the magnitude commands the current error amplifier, U8. Current feedback is provided by the internal current sense amplifier via the IOUT pin.



	TWO QUADRANT	FOUR QUADRANT	SAFE BRAKING	POWER REVERSAL	CURRENT SENSE	
					PULSE BY PULSE	AVERAGE
(a)	Yes	Yes	No	In 4-Quad Only	Yes	Yes
(b)	Yes	No	Yes	No	Yes	No
(c)	Yes	Yes	Yes	In 4-Quad Only	Yes	Yes

Figure 13. Power Stage Topologies

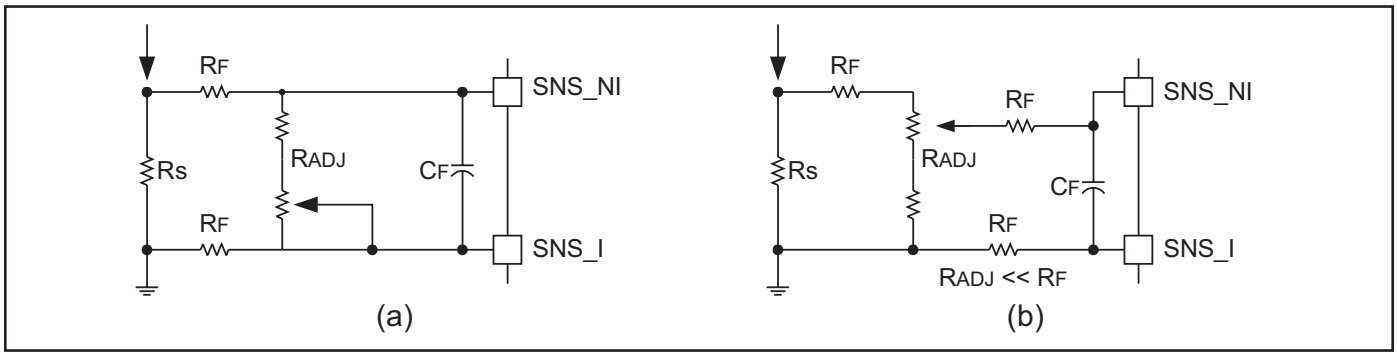


Figure 14. (a) Differential Divider and (b) Low Value Divider

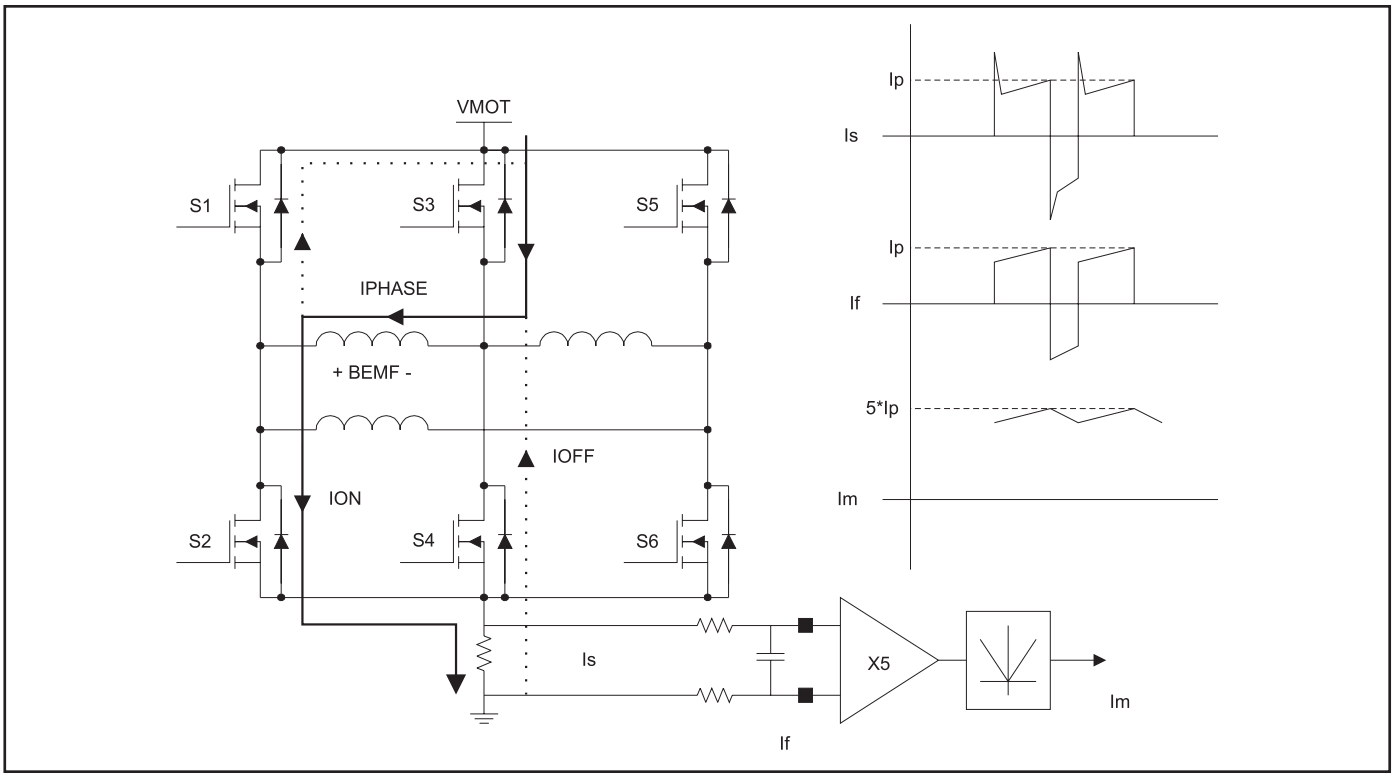


Figure 15. Current Sense Amplifier Waveform

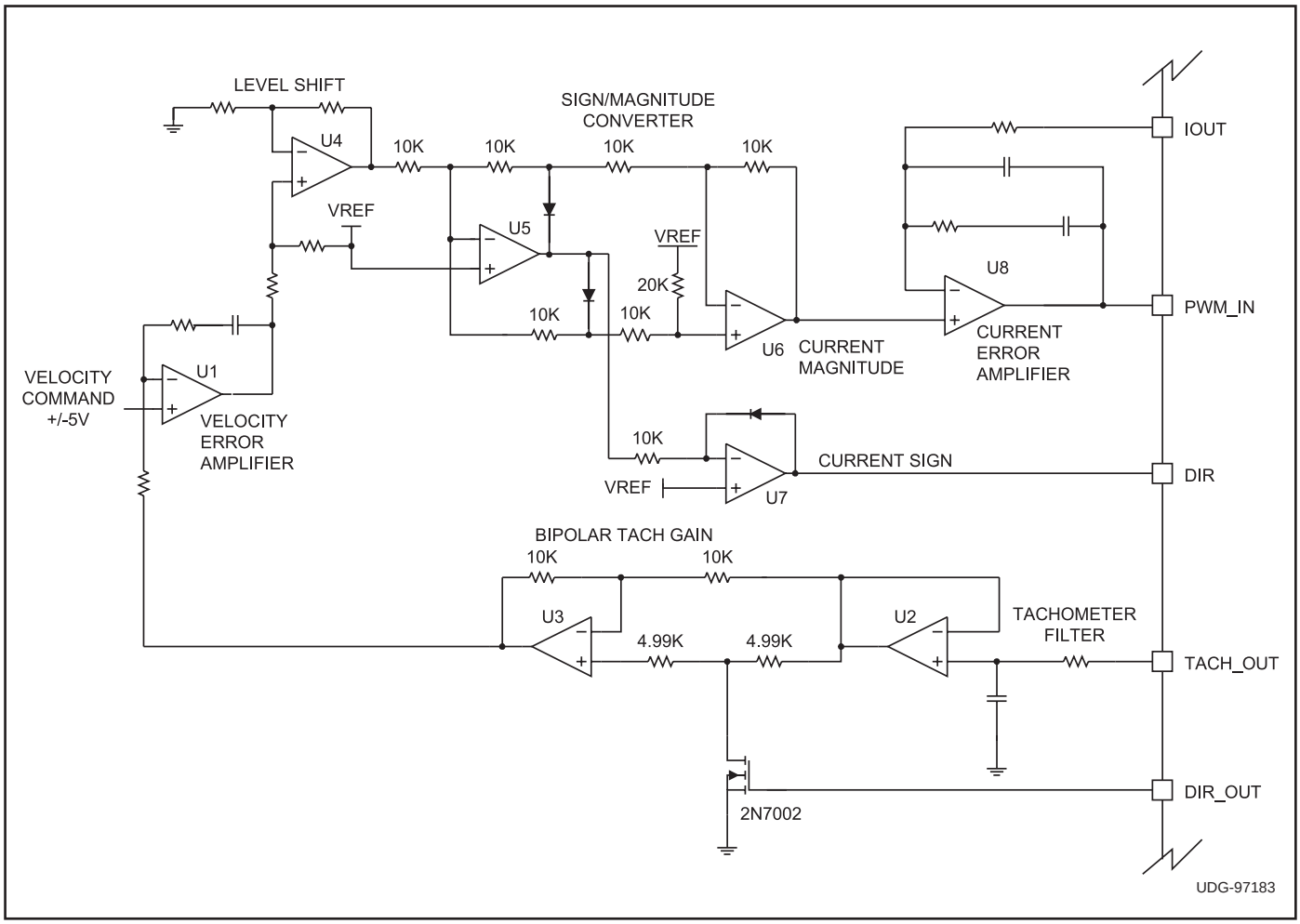


Figure 16. Four Quadrant Control Loop

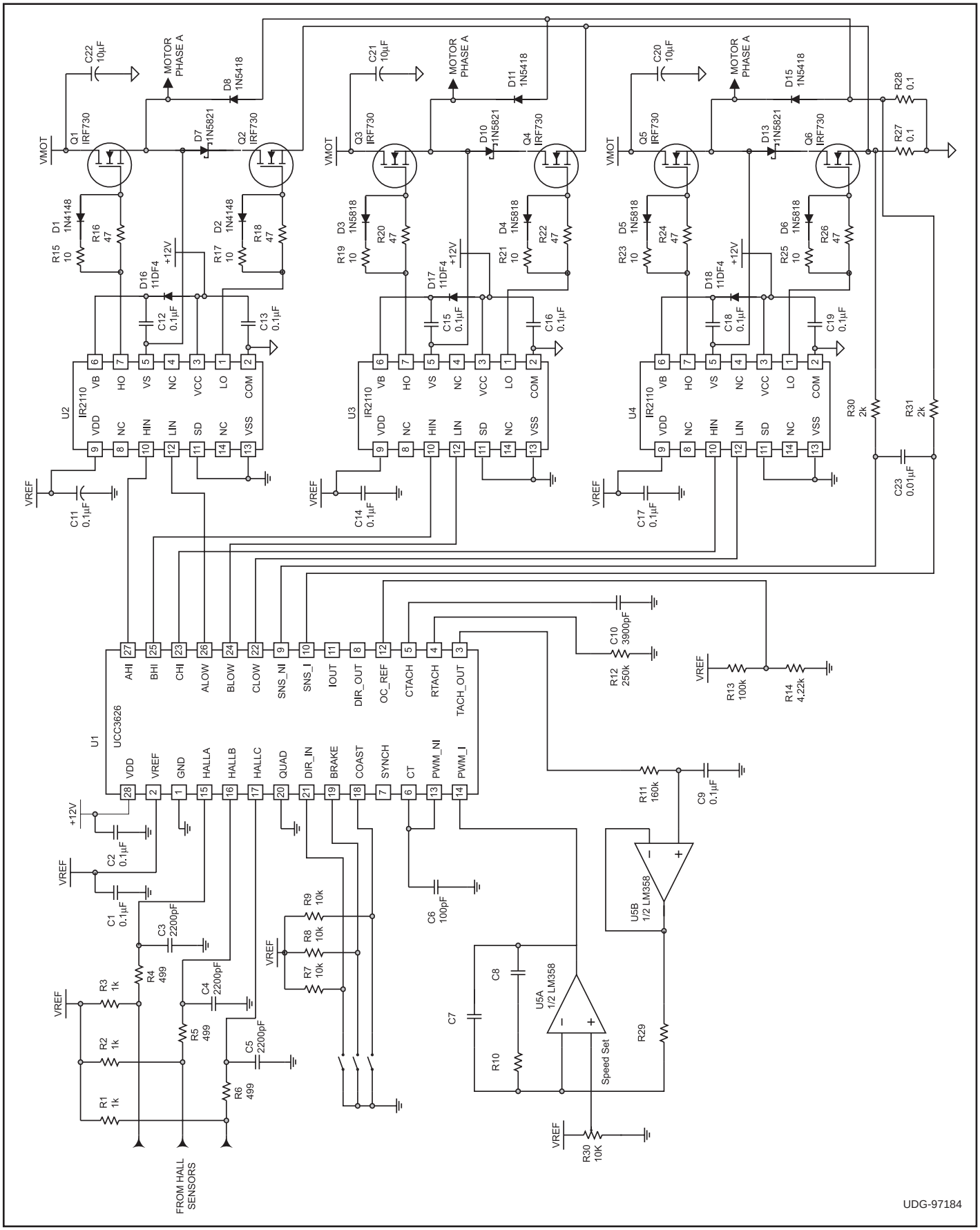


Figure 17: Two Quadrant Velocity Controller

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